

## LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. **(Currently Amended)** A memory module for ~~being inserted~~ insertion in any one of connectors formed on a motherboard, the module comprising:

a memory chip;  
a pin configured and positioned to engage with ~~for being connected to~~ the connector;  
a bus ~~for connecting~~ which connects said memory chip to said pin;  
a terminating resistor connected to one end of said bus, and  
a stab resistor connected between said pin and the other end of said bus.

2. **(Currently Amended)** A memory module as claimed in Claim 1, said connectors being connected to a memory controller in a stab connection style, said stab resistor and said terminating resistor having stab resistance  $R_s$  and terminating resistance  $R_{term}$ , respectively, wherein

said stab resistance  $R_s$  and said terminating resistance  $R_{term}$  are given by:

$$R_s = (N-1) \times Z_{effdimm} / N, \text{ and}$$

$$R_{term} = Z_{effdimm}$$

where  $N$  represents the number of said connectors; and  $Z_{effdimm}[[,]]$  represents the effective impedance of a memory chip arrangement portion consisting of said bus and said memory chip.

3. **(Original)** A memory module as claimed in Claim 1 further comprising other memory chips, wherein said bus is connected to all of the memory chips in common.

4. **(Original)** A memory module as claimed in Claim 1 further comprising other memory chips, other pins corresponding to said other memory chips respectively, and other buses for connecting said memory chips to said other pins severally.

5. **(Original)** A memory module as claimed in Claim 1, wherein said bus comprises a bi-directional bus.

6. **(Original)** A memory module as claimed in Claim 1, wherein said bus comprises a unidirectional bus.

7. **(Original)** A memory module as claimed in Claim 1, wherein said terminating resistor is formed in said memory chip.

8. **(Currently Amended)** A memory system including a plurality of memory modules inserted in connectors formed on a motherboard, wherein each of said memory module comprises:  
a memory chip;  
a pin configured and positioned to engage with one of said connectors; for being connected to the connector;  
a bus for connecting which connects said memory chip to said pin;  
a terminating resistor connected to one end of said bus, and  
a stab resistor connected between said pin and the other end of said bus.

9. **(Currently Amended)** A memory system as claimed in Claim 8, said connectors being connected to a memory controller in a stab connection style on a motherboard, said stab resistor and said terminating resistor having stab resistance  $R_s$  and terminating resistance  $R_{term}$ , respectively, wherein

said stab resistance  $R_s$  and said terminating resistance  $R_{term}$  are given by:

$$R_s = (N-1) \times Z_{effdimm} / N, \text{ and}$$

$$R_{term} = Z_{effdimm}$$

where  $N$  represents the number of said memory modules; and  $Z_{effdimm}[[,]]$  represents the effective impedance of a memory chip arrangement portion consisting of said bus and said memory chip, and wherein

said mother board has wiring impedance  $Z_{mb}$  represented by:

$$Z = (2N-1) \times Z_{effdimm}.$$

10. **(Currently Amended)** A memory system as claimed in Claim 8, wherein each of said memory modules further comprising comprises other memory chips, wherein and said bus is connected to all of the memory chips in common in each of said memory modules.

11. **(Original)** A memory system as claimed in Claim 8, each of said memory modules further comprising other memory chips, other pins corresponding to said other memory chips respectively, and other buses for connecting said memory chips to said other pins severally.

12. **(Original)** A memory system as claimed in Claim 8, wherein said bus comprises a bi-directional bus.

13. **(Original)** A memory system as claimed in Claim 8, wherein said bus comprises a unidirectional bus.

14. **(Currently Amended)** A memory system as claimed in Claim 13, wherein said connectors are connected to said memory controller in stab connection style, said stab resistor and said terminating resistor having stab resistance  $R_s$  and terminating resistance  $R_{term}$ , respectively, wherein

said stab resistance  $R_s$  and said terminating resistance  $R_{term}$  meet an equation of:

$$Z_{mb} = (R_s + Z_{effdimm}) / N$$

where  $Z_{mb}$  represents wiring impedance of said motherboard;  $Z_{effdimm}[[,]]$  represents the effective impedance of a memory chip arrangement portion consisting of said bus and said memory chip; and  $N$ , the number of said memory module modules.

15. **(Original)** A memory module as claimed in Claim 1, wherein said terminating resistor is formed in said memory chip.